TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC4024AP, TC74HC4024AF

7 - STAGE BINARY COUNTER

The TC74HC4024A is a high speed CMOS 7 - STAGE BINARY COUNTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

A negative transition on the $\overline{\text{CK}}$ input brings one increment to the counter.

A CLR input is used to reset the counter to the all low level state. A high level at CLR accomplishes the reset function.

All divided output stages are provided, and the last stage, 1/128 divided frequency will be obtained.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

• High Speed------------------------f_{MAX} = 70MHz (typ.)

at $V_{CC} = 5V$

• High Noise Immunity $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)

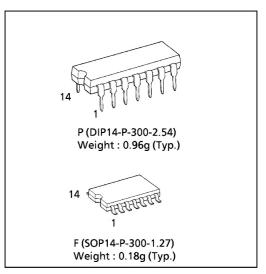
• Output Drive Capability ----- 10 LSTTL Loads

• Symmetrical Output Impedance... | I_{OH} | = I_{OL} = 4mA (Min.)

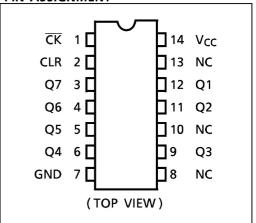
Balanced Propagation Delays ····· t_{pLH} ≃ t_{pHL}

• Wide Operating Voltage Range ···· V_{CC} (opr.) = 2V~6V

• Pin and Function Compatible with 4024B



PIN ASSIGNMENT

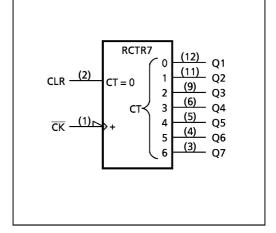


TRUTH TABLE

INPUTS		OUTDUT STATUS
CK	CLR	OUTPUT STATUS
Х	Н	ALL OUTPUTS = "L"
<u>_</u>	L	NO CHANGE
Į.	L	ADVANCE TO NEXT STAGE

X: Don't Care

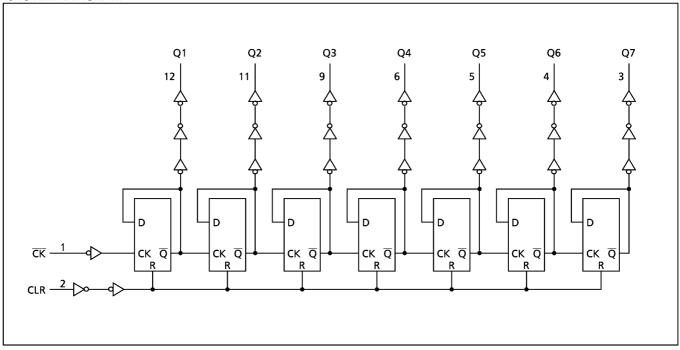
IEC LOGIC SYMBOL



961001EBA2

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SYSTEM DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	− 0.5 ~ 7	V
DC Input Voltage	V _{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V _{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I _{IK}	± 20	mA
Output Diode Current	I _{OK}	± 20	mA
DC Output Current	I _{OUT}	± 25	mA
DC V _{cc} / Ground Current	I _{cc}	± 50	mA
Power Dissipation	P _D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T _{stg}	−65~150	°C

^{*500}mW in the range of Ta= $-40^{\circ}\text{C}\sim65^{\circ}\text{C}$. From Ta=65°C to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{cc}	2~6	V
Input Voltage	V _{IN}	0~V _{cc}	V
Output Voltage	V _{OUT}	0∼V _{cc}	V
Operating Temperature	T _{opr}	−40~85	°C
Input Rise and Fall Time	t _r , t _f	$0 \sim 1000 \text{ (V}_{CC} = 2.0\text{V)}$ $0 \sim 500 \text{ (V}_{CC} = 4.5\text{V)}$ $0 \sim 400 \text{ (V}_{CC} = 6.0\text{V)}$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	YMBOL TEST CONDITION		V _{cc}	Ta = 25°C		C	Ta = −40~85°C		UNIT
FARAIVIETER	STIVIBUL	1231 CO	MOTTON	(V)	MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}				1.50 3.15 4.20	_ _ _	_ _ _	1.50 3.15 4.20	_ _ _	v
Low - Level Input Voltage	VIL			2.0 4.5 6.0		_ _ _	0.50 1.35 1.80	_ _ _	0.50 1.35 1.80	٧
High - Level Output Voltage	V _{OH} V _{IN}	V _{IN} = V _{IH} or V _{IL}	$I_{OH} = -20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	_ _ _	1.9 4.4 5.9	_ _ _	v
			$I_{OH} = -4 \text{ mA}$ $I_{OH} = -5.2 \text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	_	4.13 5.63	_	
Low - Level Output Voltage	V _{OL}		I _{OL} = 20μΑ	2.0 4.5 6.0	1 1 1	0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	v
	VIHC		$I_{OL} = 4$ mA $I_{OL} = 5.2$ mA	4.5 6.0	_	0.17 0.18	0.26 0.26	_	0.33 0.33	
Input Leakage Current	I _{I N}	$V_{IN} = V_{CC}$ or GND		6.0	ı	_	±0.1	_	± 1.0	
Quiescent Supply Current	I _{cc}	$V_{1N} = V_{C}$	_c or GND	6.0		Ė	4.0	_	40.0	μ A

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		Ta = -40~85°C	UNIT
PARAIVIETER	STIVIBUL	TEST CONDITION	$V_{CC}(V)$	TYP.	LIMIT	LIMIT	UIVIII
Minimum Pulse Width	t _{W(L)}		2.0	_	75	95	
	1 .		4.5	_	15	19	
(CK)	t _{W(H)}		6.0	_	13	16	
Minimorum Dulan Midth			2.0	_	75	95	
Minimum Pulse Width	t _{W(H)}		4.5	_	15	19	ns
(CLR)			6.0	_	13	16	
			2.0	_	25	30	
Minimum Removal Time	t_{rem}		4.5	_	5	6	
			6.0	_	5	5	
			2.0	_	6	5	
Clock Frequency	f		4.5	_	31	25	MHz
1 ' '			6.0	_	36	29	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15pF$, $V_{CC} = 5V$, $Ta = 25^{\circ}C$, Input $t_r = t_f = 6ns$)

			•	-		
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t _{TLH} t _{THL}		_	4	8	
Propagation Delay Time (CK-Q1)	t _{pLH} t _{pHL}		_	13	20	ns
Propagation Delay Time (Qn-Qn+1)	$ riangle \mathbf{t}_{\sf pd}$		_	4	9	
Propagation Delay Time (CLR—Qn)	t _{pHL}		_	13	20	
Maximum Clock Frequency	f _{MAX}		34	70	_	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

PARAMETER	CVMBOL	SYMBOL TEST CONDITION F		Ta = 25°C		C	Ta = -40~85°C		UNIT
PARAIVIETER	3 TIVIBUL	TEST CONDITION	V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	ONIT
Output Transition Time	t _{TLH}		2.0 4.5	_	30 8	75 15		95 19	
	t _{THL}		6.0	_	7	13	_	16	
Propagation Delay Time	t _{pLH}		2.0	_	60	120	_	150	
(CK-Q1)	l .'		4.5	_	16	24	-	30	
(CK-QT)	t _{pHL}		6.0	_	13	20	_	26	ns
Propagation Delay Time			2.0	_	24	60	_	75	''3
	$\triangle t_{pd}$		4.5	_	6	12	-	15	
(Qn-Qn+1)	"		6.0	_	5	10	-	13	
Propagation Delay Time			2.0	_	50	120	_	150	
	t _{pHL}		4.5	_	16	24	-	30	
(CLR — Qn)	'		6.0	_	13	20	-	26	
			2.0	6	17	_	5	_	
Maximum Clock Frequency	f _{MAX}		4.5	31	63	_	25	_	MHz
	- IVIAX		6.0	36	73	_	29	_	
Input Capacitance	C _{IN}			_	5	10	_	10	ne
Power Dissipation Capacitance	C _{PD} (1)			_	36	_	_	_	pF

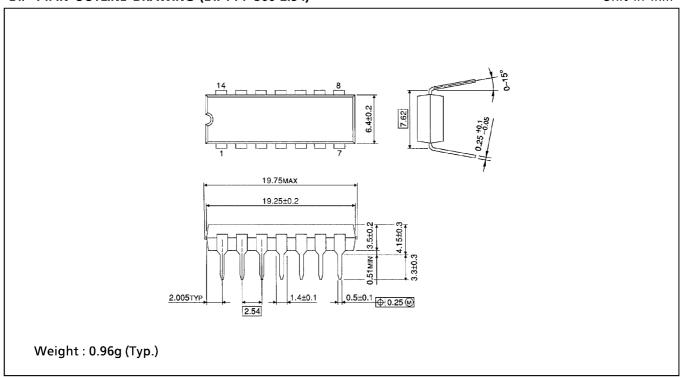
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 I_{CC} (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54)

Unit in mm



SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)

Unit in mm

